Doc Code: AP.PRE.REQ

PTO/SB/33 (09-08)
Approved for use through 10/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE



| PRE-APPEAL BRIEF REQUEST FOR REVIEW | Docket Number (Optional) SON-2815 | |
|---|---|---|
| | Application Number 10/525,203-Conf. #7661 | Filed February 22, 2005 |
| | First Named Inventor Yuichi Takagi et al. | |
| | Art Unit 2629 | Examiner D. P. Joseph |

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant /inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☒ attorney or agent of record.
Registration number 40,290 / 24,104

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34. _____

40,290
Signature

Christopher M. Tobin
Ronald P. Kananen
Typed or printed name

(202) 955-3750
Telephone number

October 22, 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of 1 forms are submitted.

Docket No.: SON-2815
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:
Yuichi Takagi et al.

Application No.: 10/525,203 | Confirmation No.: 7661

Filed: February 22, 2005 | Art Unit: 2629

For: CURRENT OUTPUT TYPE DRIVE CIRCUIT AND DISPLAY DEVICE | Examiner: D. P. Joseph

## REQUEST FOR PRE-APPEAL BRIEF PANEL REVIEW

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This request for Pre-Appeal Panel Review is in response to the Final Office Action dated May 30, 2008 and received in this application. Applicant has concurrently filed a Notice of Appeal regarding all outstanding grounds of rejection and will file an Appeal Brief in due course. However, it is anticipated that Panel Review will obviate the need for the filing a Brief.

Due to the space constraints imposed in presenting Applicant's position, various claims are referenced below, but cannot be fully reproduced. The pending claims are of record and are reflected in the listing of claims in the previously filed Request for Reconsideration. It is believed that actual appreciation of the claims will result in a conclusion that various rejections of independent and dependent claims as noted below merit reversal, in light of the following remarks.

Claims 1-28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,332,661 to Yamaguchi ("Yamaguchi") in view of U.S. Pat. No. 7,180,496 to Koyama et al. ("Koyama"). This rejection is traversed.

Referring first to independent claim 1, these claimed features are neither disclosed nor suggested by the relied-upon references. Yamaguchi discloses a constant current driving semiconductor integrated circuit configured to drive several loads by using a reference current generating circuit that is embedded to derive a reference output current generated on a reference resistance from a reference output terminal.

Koyama discloses a line driver circuit that outputs digital values (D1, D2, D3) to the pixel array in the form of a voltage. As admitted in the Action, Yamaguchi fails to disclose "*a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means.*" Nor does Koyama. Elements 201 and 202 are a purported example of this feature, but these elements merely accommodate a latching of a digital signal (D1, D2, D3) that is then provided to a pixel circuit 205. Even if this is construed as "sampling" and "holding", the passing of a digital value D1, D2, or D3 to another circuit is clearly not an example of sampling a reference current input from a reference current input terminal.

Additionally, and contrary to the conclusory remarks of the Examiner that sampling and holding signals is a known technique and that this combination would have been obvious, one of ordinary skill in the art would not have combined the claimed elements by known methods as there would be no technical impetus whatsoever to make the modifications consistent with Applicant's claimed invention, and there would thus also be no expectation that success would result in adding such features to the circuitry of Yamaguchi.

FIG. 1 of Yamaguchi illustrates current driving circuitry. Yamaguchi also describes circuitry that provides a current mirror circuit including transistors configured to produce reference current outputs OREF1-3 that have small variations in current value. (See FIG. 3 of Yamaguchi). It would make no technical sense whatsoever to sample and hold these currents in the Yamaguchi circuitry, as these currents are intended to drive loads (with the alleged small variation in current). If one were to sample and hold the OREF1-3 currents, in lieu of using them to drive loads, the circuitry would be rendered completely non-functional. The reference to FIG. 2 of Yamaguchi (Office Action, at p. 21) as further evidence of the propriety of the combination only further

highlights the specious nature of the rejection. Although the explanation in the reference is scant, the register and latch disclosed therein are apparently control circuitry used to determine which line the drive current is to be applied to. This has nothing to do with sampling or holding the value of the actual current.

Accordingly, Yamaguchi discloses circuitry for producing several drive currents with small variation, and Koyama discloses an entirely different type of circuit and fails to disclose or in any way suggest the claimed features that the Action admits are absent from the Yamaguchi reference. The line (voltage) driver circuit by Koyama is a clearly distinct from the current driver circuit claimed by Applicant. An ordinarily skilled artisan would in no way look to the latching of a digital value (D1-D3) for application to a line in a pixel circuit to solve problems presented in the current drive circuitry of Yamaguchi. Regardless, a *prima facie* case of obviousness remains absent from the record as even the combination of references would still fail to yield the features of Applicant's claimed invention, namely "*a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means*." For these reasons, the combination of references is thus deficient generally, and the faulty combination still fails to produce the features recited in Applicant's claim 1.

The position with regard to various dependent claims and other independent claims in the Action only further illustrates the impropriety of the combination as well as the deficiencies of the references, even in combination.

For example, regarding claim 3, the Action cites elements A1 to A3 and B1 to B3 as the first current memory and elements C1 to C3 as the second current memory. However, these elements are part of the pixel, not a part of the line drive circuit. It is clear that these features are not an example of first and second current memories in a current sampling circuit, let alone those that alternately perform write and read operations as claimed. Again, Applicant's claimed invention provides two memory circuits to write and read the reference current in the reference current source circuit, not within the pixel array. The second current memory C1-C3 is merely a non-volatile memory that stores the values in the given pixel when power to the display is cut off, so that the display can automatically display something when it is turned back on. The other elements A1 to

A3 and B1 to B3 are merely faster, volatile memories for accommodating a refresh of the display. It is difficult to see how the cited features of Koyama have anything at all to do with the features recited in Applicant's claim 3. Applicant calls the claimed first and second memories to be a "design choice" in the Advisory Action, but this is certainly objected to. Applicant more than generically claims these memories as they are assigned recited roles writing and reading the reference circuit in the current sampling circuit, as noted. This feature is being ignored in the Action.

Still further, with regard to claim 4, the relied-upon references offer no disclosure or suggestion of means for increasing the reference current read from the current memory via distribution by time division. It is not sufficient to state that time division is known, as there would be no reason to distribute reference currents by time division in the Yamaguchi reference. With regard to claim 5, there is clearly no disclosure or suggestion of the additional features for carrying out such an operation as clamed. Applicant objects to the unsupported conclusory statements that these claimed features are obvious.

With regard to claim 6, there is also absolutely no discussion in Yamaguchi, as alleged in the Action, of distributing the reference current to the drivers in a vertical blanking period, or of using as the reference current the current held after the vertical blanking period in which digital noise is generated, as claimed by Applicant. Even assuming that Yamaguchi column 6, lines 22-45 discloses the usage of clock signals to control displayed information, there is no mention or suggestion of any kind of distributing the reference current to the drivers in a vertical blanking period. It would also make no sense to do this in Yamaguchi as that circuitry provides drive currents for driving loads. There is no way one would in any way think that it would be "inherent" to distribute the reference current in a vertical blanking period, as this would be non-functional in the Yamaguchi reference. Applicant objects to the unsupported conclusory statement that these claimed features would have been obvious. The conclusory statements in the Advisory Action repeat more of the same, but Applicant reiterates that the features of claim 6 are clearly wholly absent from the reference.

Independent claim 7 is distinct from the relied-upon references for the reasons noted regarding claim 1 above, but the claim adds additional features that are also not disclosed. For example, the references do not disclose (1) connecting the reference current inputs according to a common current interconnect, or of (2) distributing the reference current to the reference current source circuits of the drivers by time division. As explained above, Yamaguchi discloses a reference current generating circuit that is embedded to derive a reference output current generated on a reference resistance from a reference output terminal. FIG. 3 of Yamaguchi discloses its reference current generating circuit, which is explicitly described as producing different currents for the different current driver circuits. This is not an example of the common current interconnect claimed by Applicant. In any event, there is clearly no distribution of the reference current to the reference current source circuits of the drivers by time division, nor is there anything that could coherently support a conclusion that there is any hint or suggestion in that regard. The use of time division appears wholly inappropriate to the circuitry of Yamaguchi, and it is unclear how or if Yamaguchi's drive circuitry would function under such a scenario. In any case, there is clearly no indication whatsoever that time division would be used in the context or fashion claimed by Applicant. It is wholly insufficient to merely conclude that time division is known, and that therefore it would be obvious. Koyama also fails to disclose or in any way suggest such features. The passage cited in the Action, spanning lines 1-21 in column 10, discloses a gray scale technique, which also clearly does not disclose or suggest the claimed features.

Accordingly, Applicant respectfully requests reversal of the rejection of claims 1-28 under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi in view of Koyama.

Dated: October 22, 2008

Respectfully submitted,

By _____ 40,290

Ronald P. Kananen
Registration No.: 24,104
Christopher M. Tobin
Registration No.: 40,290
RADER, FISHMAN & GRAUER PLLC
Correspondence Customer Number: 23353
Attorneys for Applicant